AMENDMENTS TO THE SPECIFICATION

IN THE ABSTRACT OF THE DISCLOSURE:

Replace the Abstract of the Disclosure currently of record with the attached new Abstract of the Disclosure.

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IN THE SPECIFICATION:

Please amend the paragraph beginning on page 3, line 10, as follows:

--As shown in Fig. 1, the Ethernet switch basically comprises of switch integrated circuit 100 and several port integrated circuits 110a, 110b, and 110c. The switch integrated circuit 100 controls the delivery and switch of network packets among ports. Port integrated circuits 110a, 110b, and 110c comprise internal memories 120a, 120b , and 120c for saving and switching network packets. Under this Ethernet framework, when a network packet is to be transmitted from port [[120a]] 130a to port [[130c]] 130b, the packet has to be first saved in the memory 120a, then transported from the memory 120a to the memory 120c. Therefore, the operating performance of this Ethernet switch is not promising. In addition, to enable the links of various LANs, such as 100BASE5, 10BASE2, 10BASE-T, 100BASE-TX, 100BASE-T4, or 100BASE-FX this type of Ethernet switch requires external memory, which is an additional cost.--

Please amend the paragraph beginning on page 4, line 6, as follows:

--To realize the above and other objects, this invention provides an Ethernet switch for selectively transporting or filtering network packets. The Ethernet switch of this invention

comprises plural network ports, a first and a second memory device, a first and a second memory control devices, an switch device, and a [[second]] memory management device. Network ports are for receiving or delivering network packets. The first memory device saves the source address and associates messages of the network packets. The second memory device saves the network packets received from the network port. The first and the second memory control devices connect to the first and the second memory devices, respectively, for controlling the read and write of the first and the second memory devices. Further, the switch device connects the network port and the first memory control device, for creating a source address and the associated messages of the network port for each network packet, and for creating a destination address and the associated messages of the network port for each network packet in accordance with the contents of the first memory device for managing the contents of the first memory device. The second memory device connects the network port and the second memory control device for managing the contents of the second memory device.--

Please amend the paragraph beginning on page 7, line 11, as follows:

--To realize the above and other objects, this invention provides an Ethernet switch, for selectively transporting or filtering network packets. The Ethernet switch of this type

comprises plural network ports, a first and a second memory device, a first and a second memory control devices, a switch device, and a [[second]] memory management device. Network ports are for receiving or delivering network packets. The first memory device saves the source address and associated messages of the network packets. The second memory device saves the network packets received from the network port. The first and the second memory control devices connect to the first and the second memory devices, respectively, for controlling the read and write of the first and the second memory devices. Besides, the switch device connects the network port and the first memory control device, for creating a source address and the associated messages of the network port for each network packet, and for creating a destination address and the associated messages of the network port for each network packet in accordance with the contents of the first memory device for managing the contents of the first memory device. The second memory device connects the network port and the second memory control device for managing the contents of the second memory control device for managing the contents of the second memory device. The shared memory access control circuit controls the access to the shared memory device. An embodiment of this invention is specified in detail with reference to the drawing as follows.--